Connect Tech Inc.

Embedded Computing Experts

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USERS GUIDE

FreeForm/PCI-104

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Preface

Disclaimer

The information contained within this user's guide, including but not limited to any product specification, is subject to change without notice.

Connect Tech assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and the user's guide.

Customer Support Overview

If you experience difficulties after reading the manual and/or using the product, contact the Connect Tech reseller from which you purchased the product. In most cases the reseller can help you with product installation and difficulties.

In the event that the reseller is unable to resolve your problem, our highly qualified support staff can assist you. Our support section is available 24 hours a day, 7 days a week on our website at: http://connecttech.com/support/resource-center/. See the contact information section below for more information on how to contact us directly. Our technical support is always free.

Contact Information

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Note:
Please go to the **Connect Tech Resource Center** for product manuals, installation guides, device drivers, BSPs and technical tips. Submit your **technical support** questions to our support engineers.

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Technical Support representatives are ready to answer your call Monday through Friday, from 8:30 a.m. to 5:00 p.m. Eastern Standard Time. Our numbers for calls are:

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You may obtain warranty service by delivering this product to an authorized Connect Tech Inc. business partner or to Connect Tech Inc. along with proof of purchase. Product returned to Connect Tech Inc. must be pre-authorized by Connect Tech Inc. with an RMA (Return Material Authorization) number marked on the outside of the package and sent prepaid, insured and packaged for safe shipment.

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ESD Warning

Electronic components and circuits are sensitive to ElectroStatic Discharge (ESD). When handling any circuit board assemblies including Connect Tech COM Express carrier assemblies, it is recommended that ESD safety precautions be observed. ESD safe best practices include, but are not limited to:

- Leaving circuit boards in their antistatic packaging until they are ready to be installed.
- Using a grounded wrist strap when handling circuit boards, at a minimum you should touch a grounded metal object to dissipate any static charge that may be present on you.
- Only handling circuit boards in ESD safe areas, which may include ESD floor and table mats, wrist strap stations and ESD safe lab coats.
- Avoiding handling circuit boards in carpeted areas.
- Try to handle the board by the edges, avoiding contact with components.

Revision History

Revision	Date	Changes
0.09	2018-07-16	Updated format; Updated dev kit references

Introduction

Connect Tech's FreeForm/PCI-104 features Xilinx's Virtex-5 multi-platform FPGA offering users a flexible, reconfigurable computing platform that also takes advantage of the high bandwidth capabilities of the PCI bus while communicating with various I/O interfaces.

Product Features

- PCI-104 form factor – 32-Bit/33MHz, both 3.3V and 5V signaling are supported
- Xilinx multi-platform Virtex-5 FPGA with 3 million logic gates
- 2 or 4 MB Flash for FPGA configuration storage
- 8MB Flash for embedded code storage
- Designed for embedded processing using MicroBlaze™
- 100MHz input clock
- 128MB DDR2-400 memory
- 2 x 10/100 Ethernet with modular jacks
- 2 x RS-485 serial interface
- High-speed serial connector 4 x Rocket I/O (GTP) channels
- 64 single ended or 32 LVDS general purpose I/O
- External 5V power connection for programming and development
- JTAG test and programming chain
- Industrial temperature range of -40°C to 85°C
- Ships preconfigured with a reference design

About this manual

This manual will provide the user with the following information:

- System overview
- Introduction to the reference design
- Description of jumpers, switches, and connector pinouts
- Hardware installation instructions
- Software installation instructions
- FPGA configuration details
- Specifications

System Overview

The following conceptual block diagram provides a high level overview of the FreeForm/PCI-104 and illustrates the general interconnection between components and connectors.

For the actual orientation and description of components refer to Figure 2 and Table 1 respectively.

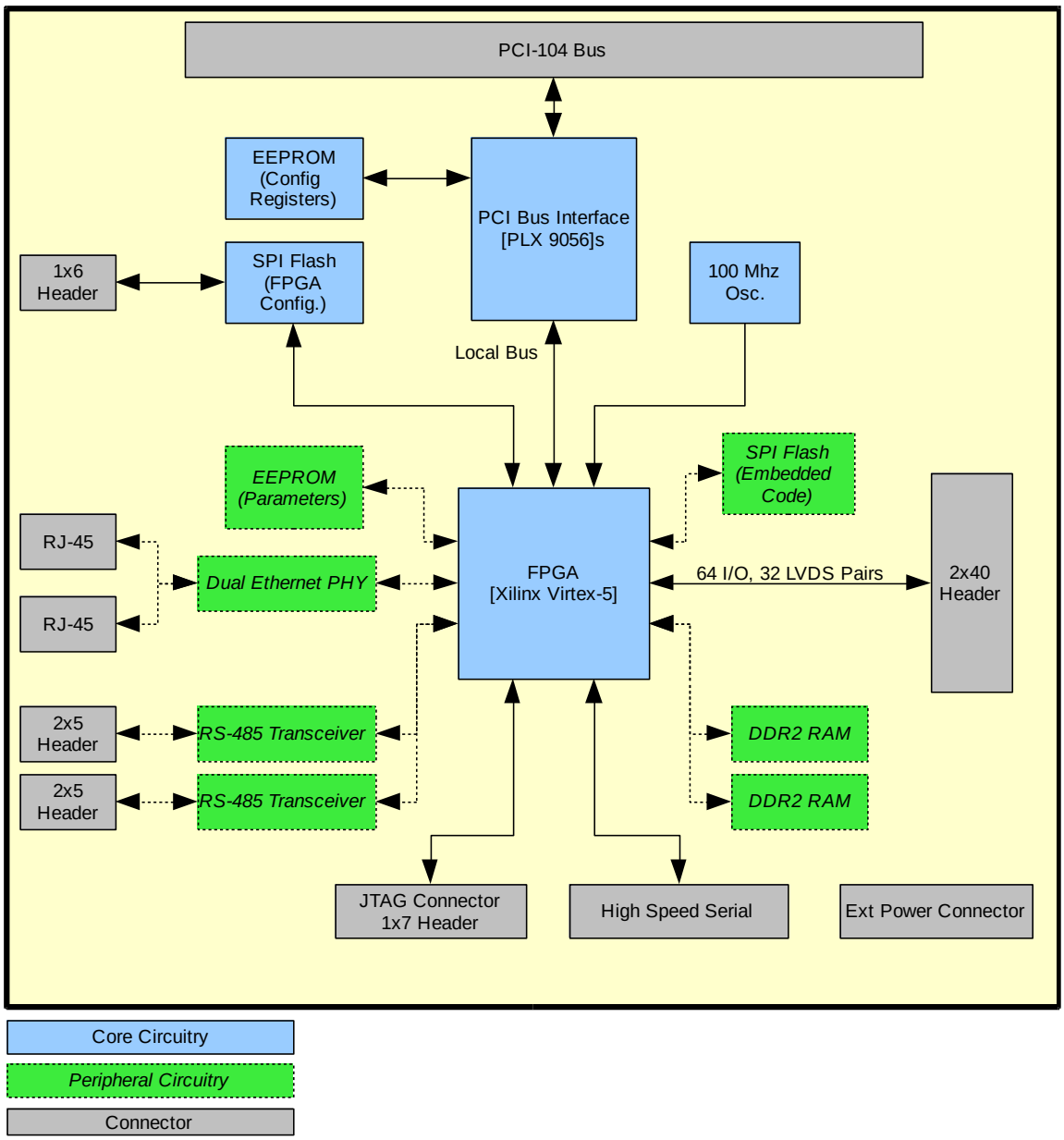


Figure 1: FreeForm/PCI-104 Block Diagram

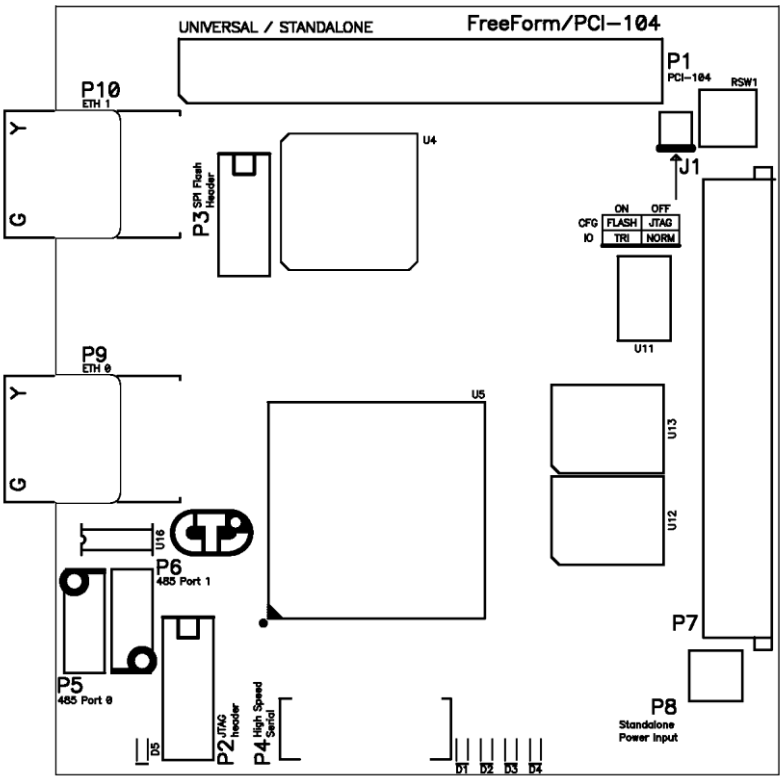


Figure 2: FreeForm/PCI-104 Layout

Table 1: FreeForm/PCI-104 Components

Connectors	Description
P1	PCI-104 connector
P2	JTAG programming header
P3	SPI flash programming header
P4	High-speed serial connector
P5, P6	RS-485 header
P7	GPIO header
P8	External power header
P9	RJ-45 A
P10	RJ-45 B
Jumpers /Switches	**Description**
RSW1	Slot selection
J1	FPGA configuration settings
Components	**Description** *(not all on top side)*
D1-D4	User LEDs
D5	FPGA load complete LED
U4	PLX PCI-local bus bridge
U5	Virtex-5 FPGA
U10	FPGA configuration flash
U11	Embedded code flash
U12, U13	DDR2 memory
U14	Parameter EEPROM
U15, U16	RS-485 transceiver

U17	Dual 10/100 PHY
O1,O2, O3	Oscillators

Reference Design

The FreeForm/PCI-104 ships with a pre-installed reference design that is loaded into the FPGA's configuration flash. This reference design demonstrates how to interface the FreeForm/PCI-104 (Virtex-5 FPGA) with the PLX PCI 9056 PCI to Local Bus Bridge, as well as the various peripherals.

The PLX 9056 provides a generic local bus that is capable of operating at up to 66MHz (this design forwards a 50MHz clock to the PLX). The PLX bridge has been set in the C-Mode of operation. The reference logic operates as a local bus slave, as well as a local bus master.

The reference design contains examples demonstrating:

- Loading of PLX 9056's registers via the local bus
- Local bus slave transfers
- Local bus master transfers
- GPIO control
- Programming the SPI Flash
- Interfacing to the built-in Virtex-5 TEMACs
- RS-485 serial data transfers
- Reading/writing to the serial EEPROM
- Reading/writing to DDR2 memory
- Interfacing to the Virtex-5 Rocket I/O transceivers

Most of the example VHDL modules demonstrate how to interface with the various peripherals through a register set, which is accessible by the host system over the PCI bus. A set of software applications has been created to show how the host system can communicate with each FPGA sub-module. In most applications, the host system will not directly control these peripherals. In a custom application, these modules can be easily modified to interconnect with each other through the FPGA fabric.

To obtain the source code, refer to Software Installation. For further details on the reference design, refer to *FreeForm/PCI-104 Reference Design Guide (CTIM-00042)*

Hardware Description

The following sections describe the function of all switches/jumpers and provide details on connector pinouts.

Jumpers and Switches

Slot Selection (RSW1)

This rotary switch selects a slot position in the PCI-104 stack. When mounting on a PCI adapter card, ensure slot one is selected.

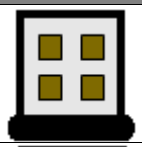
Table 2: Slot Selection (RSW1)

Position	Slot
0,4	0
1,5	1
2,6	2
3,7	3

FPGA Configuration Settings (J1)

Jumper J1 is used to control FPGA configuration.

Table 3: FPGA Configuration Settings (J1)

Location	Function
	FPGA waits for configuration over JTAG (using P2)
	FPGA reads configuration from SPI flash
	FPGA is tri-stated, flash is isolated from FPGA and can be programmed directly

Connector Pinouts

PCI-104 Header (P1)

Refer to PCI-104 specifications.

Note: The FreeForm/PCI-104 only requires the 5V power supply,. The board is compatible with PCI-104 mother boards that supply just 5V or both 3.3V & 5V.

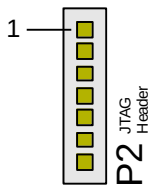
JTAG Programming Header (P2)

Use P2 to configure the FPGA via JTAG. Refer to FPGA Configuration for more information. Power pins are for voltage reference only; they do not provide power to the configuration circuitry.

Note that the FPGA can always be programmed via JTAG, regardless of the J1 configuration setting.

Table 4: JTAG Programming Header Pinout (P2)

Pin	Signal	Direction
1	TRST	Input
2	TMS	Input
3	TDI	Input
4	TDO	Output
5	TCK	Input
6	GND	Reference
7	3.3V	Reference



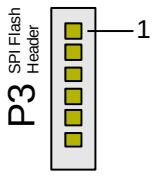
Top View

SPI Flash Programming Header (P3)

P3 may be used to directly program the SPI flash, providing that J1 is set correctly to the tri-state FPGA position. The power pins are for voltage reference only. They do not provide power to the configuration circuitry.

Table 5: SPI Flash Programming Header Pinout (P3)

Pin	Signal	Direction
1	SPI_CSN	Input
2	SPI_MOSI	Input
3	SPI_MISO	Output
4	SPI_CLK	Input
5	GND	Reference
6	3.3V	Reference



Top View

High-speed Serial (P4)

The high-speed serial connector carries four Rocket (GTP) I/O channels, each with a dedicated transmit and receive differential pair. These channels are capable of operating up 3.125 Gbps, depending on configuration. For more information on Rocket I/O capabilities, visit the Xilinx website: http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/

Table 6: High-Speed serial Connector Pinout (P4)

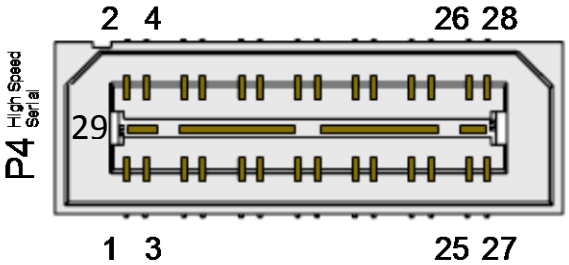
Pin	Signal	Direction	Notes
1	MTGRXN0_112	Input	(b)
3	MTGRXP0_112	Input	(b)
2	MTGTXN0_112	Output	(b)
4	MTGTXP0_112	Output	(b)
5	HSS_USER_IO(0)	Input/Output	(a), (d)
7	HSS_USER_IO(1)	Input/Output	(a), (d)
6	HSS_USER_IO(2)	Input/Output	(a), (d)
8	HSS_USER_IO(3)	Input/Output	(a), (d)
9	MTGRXN1_112	Input	(b)
11	MTGRXP1_112	Input	(b)
10	MTGTXN1_112	Output	(b)
12	MTGTXP1_112	Output	(b)
13	3.3V	Power	(a)
15	3.3V	Power	(a)
14	3.3V	Power	(a)
16	3.3V	Power	(a)
17	MTGRXN0_114	Input	(c)
19	MTGRXP0_114	Input	(c)
18	MTGTXN0_114	Output	(c)
20	MTGTXP0_114	Output	(c)
21	3.3V	Power	(a)
23	3.3V	Power	(a)
22	3.3V	Power	(a)
24	3.3V	Power	(a)
25	MTGRXN1_114	Input	(c)
27	MTGRXP1_114	Input	(c)
26	MTGTXN1_114	Output	(c)
28	MTGTXP1_114	Output	(c)
29	GND	Power	(f)
30	GND	Power	(f)
31	GND	Power	(f)
32	GND	Power	(f)

Notes:

a) Pins have a different function from Revision B.
b) The Rocket I/O (GTP) are organized into tiles, where each tile has two transceivers and shares a common PLL. In this design, tiles 112 and 114 are used.
c) Tile 112 has AC coupling capacitors on the TX pairs, validated at PCI Express data rates (2.5 Gbps).
d) Tile 114 has AC coupling capacitors on both the RX and TX pairs, validated at SATA data rates (1.5 Gbps).
e) HSS_USER_IO are flexible LVCMOS side-band signals.
f) Pins 29-32 are the ground blades running down the center of the high speed connector

WARNING	If connecting two FreeForm/PCI-104's together using the Rocket I/O interface in a cross-over fashion; care must be taken when building a custom Samtec EQDP cable. Special considerations are required when connecting a FreeForm/PCI104 Rev B to later revisions. See Appendix C: Hardware Changes from Revision B.

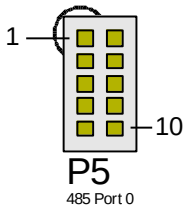
Top View



RS-485 Headers (P5, P6)

Table 7: RS-485 Port 1 Pinout (P5)

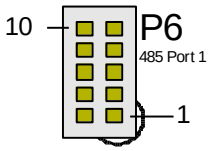
Pin	Signal	Direction
1	RXD+1	Input
2		
3	RXD-1	Input
4		
5	TXD+1	Output
6		
7	TXD-1	Output
8		
9	GND	Power
10		



Top View

Table 8: RS-485 Port 2 Pinout (P6)

Pin	Signal	Direction
1	RXD+2	Input
2		
3	RXD-2	Input
4		
5	TXD+2	Output
6		
7	TXD-2	Output
8		
9	GND	Power
10		



Top View

GPIO Header (P7)

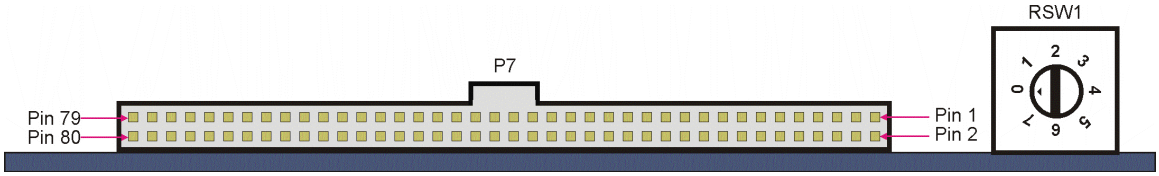
When in differential mode, the GPIO header positive (P) and negative (N) signals are adjacent on a standard ribbon cable. Note that the GPIO voltage level is set via hardware.

- FCG001: L12 populated, enabling 2.5V I/O, including LVDS
- FCG002: L13 populated, enabling 3.3V I/O

Table 9: GPIO Header Pinout

Pin	Signal	Direction	Pin	Signal	Direction
1	GPION(0)	Input/Output	41	GPION(16)	Input/Output
2	GPIOP(0)	Input/Output	42	GPIOP(16)	Input/Output
3	GPION(1)	Input/Output	43	GPION(17)	Input/Output
4	GPIOP(1)	Input/Output	44	GPIOP(17)	Input/Output
5	GPION(2)	Input/Output	45	GPION(18)	Input/Output
6	GPIOP(2)	Input/Output	46	GPIOP(18)	Input/Output
7	GPION(3)	Input/Output	47	GPION(19)	Input/Output
8	GPIOP(3)	Input/Output	48	GPIOP(19)	Input/Output
9	GND	Power	49	GND	Power
10	GND	Power	50	GND	Power
11	GPION(4)	Input/Output	51	GPION(20)	Input/Output
12	GPIOP(4)	Input/Output	52	GPIOP(20)	Input/Output
13	GPION(5)	Input/Output	53	GPION(21)	Input/Output
14	GPIOP(5)	Input/Output	54	GPIOP(21)	Input/Output
15	GPION(6)	Input/Output	55	GPION(22)	Input/Output
16	GPIOP(6)	Input/Output	56	GPIOP(22)	Input/Output
17	GPION(7)	Input/Output	57	GPION(23)	Input/Output
18	GPIOP(7)	Input/Output	58	GPIOP(23)	Input/Output
19	GND	Power	59	GND	Power
20	GND	Power	60	GND	Power
21	GPION(8)	Input/Output	61	GPION(24)	Input/Output
22	GPIOP(8)	Input/Output	62	GPIOP(24)	Input/Output
23	GPION(9)	Input/Output	63	GPION(25)	Input/Output
24	GPIOP(9)	Input/Output	64	GPIOP(25)	Input/Output
25	GPION(10)	Input/Output	65	GPION(26)	Input/Output
26	GPIOP(10)	Input/Output	66	GPIOP(26)	Input/Output
27	GPION(11)	Input/Output	67	GPION(27)	Input/Output
28	GPIOP(11)	Input/Output	68	GPIOP(27)	Input/Output
29	GND	Power	69	GND	Power
30	GND	Power	70	GND	Power
31	GPION(12)	Input/Output	71	GPION(28)	Input/Output
32	GPIOP(12)	Input/Output	72	GPIOP(28)	Input/Output
33	GPION(13)	Input/Output	73	GPION(29)	Input/Output
34	GPIOP(13)	Input/Output	74	GPIOP(29)	Input/Output
35	GPION(14)	Input/Output	75	GPION(30)	Input/Output
36	GPIOP(14)	Input/Output	76	GPIOP(30)	Input/Output
37	GPION(15)	Input/Output	77	GPION(31)	Input/Output
38	GPIOP(15)	Input/Output	78	GPIOP(31)	Input/Output
39	GND	Power	79	GND	Power
40	GND	Power	80	GND	Power

Side View



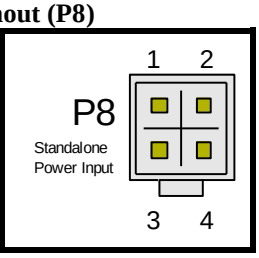
External Power Connector (P8)

The external connector provides 5V to the power regulation circuitry.

The external power connector should only be used when the FreeForm/PCI-104 is being programmed outside of a PCI/PCI-104 system.

Table 10: External Power Connector Pinout (P8)

Pin	Signal	Direction
1	5V	Power
2		
3	GND	Power
4	VIO (connect to 5V)	Power



It is recommended that a Connect Tech Inc. FreeForm/PCI-104 power supply is used for providing external power. Orientation of the power supply connector is important. Ensure that the clip on the cable aligns with the catch on P8, as shown below.

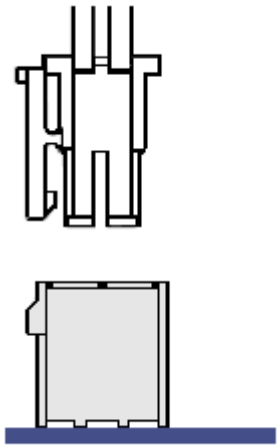


Figure 3: External Power Connection

Connector's Mating Components and Cables

The following table lists the manufacturer and part number for connectors on the FreeForm/PCI-104, as well as potential mating components.

Table 11: Connector Mate Listing

Connector	Component on FreeForm/PCI-104	Mating components	Mating cable assembly
P2	Samtec TSW-107-07-L-S (0.100" pitch, 1x7)	Samtec SSW-107-xx-G-S (Socket, other options available)	Connect Tech Inc. CBG303 (JTAG programming cable)
P3	Samtec TSW-106-07-L-S (0.100" pitch, 1x6)	Samtec SSW-106-xx-G-S (Socket, other options available)	Connect Tech Inc. CBG303 (JTAG programming cable)
P4	Samtec QSE-014-01-L-D-DP-A (0.8mm pitch, 2x14, arranged as 14 differentials pairs)	Samtec QTE-014-01-L-D-DP-A (5mm mated height, other heights available)	Samtec EQDP [Note 2]
P5/P6	Samtec TSW-105-07-L-D (0.100" pitch, 2x5)	Samtec SSW-105-xx-G-D (Socket, other options available)	Connect Tech Inc. CAG104 (Header to DB9)
P7	Tyco 5-104069-3 (0.050"x0.100" pitch, 2x40)	Tyco 3-111196-3 (ribbon cable mate) *or* Tyco 8-487937-0 (discrete wire housing) Tyco 1-487547-1 (crimps for housing)	-
P8	Samtec IPL1-102-01-S-D (0.100" pitch, 2x2)	Samtec IPD1-02-D (discrete wire housing) Samtec CC79L-2024-01-S (crimps for housing) *or* Samtec MMSD-02-22-S-03-25-S (pre-assembled housing and wiring)	Connect Tech Inc. MSG037 (5V power supply, for development purposes)

Note:
[1] CBG303 and MSG037 are available as part of development kit DEV017
[2] Connect Tech does not carry stock of the Samtec EQDP cable. The EQDP has many options, allowing for a configuration to meet the specific application. Care must be taken when selecting these options, to ensure the correct connectivity between boards.

Hardware Installation

Before installing the FreeForm/PCI-104 into a PCI-104 stack, ensure the following:

- Slot selection is properly set using the rotary switch RSW1.
- FPGA configuration jumper J1 is set to read from flash.

Once installed in the system and power is applied, the LED D1 will illuminate to indicate that FreeForm/PCI-104 is functioning.

Heat Sink Installation

Each FreeForm/PCI-104 ships with a FPGA heat sink (27 mm x 27 mm); to be installed by the user. Simply peel of the sticker backing and press firmly onto the FPGA, using proper ESD precautions.

If the heat sink size is not suitable for your application, please contact Connect Tech Inc.

WARNING	In many applications, including high speed memory operations, the FPGA dissipates a significant amount of power. Failure to use any heat sinking will result in the product warranty being voided.

Stand-alone Operation

Operating the FreeForm/PCI-104 outside of a PCI-104 stack or a PCI system for extended periods of time is not recommended. The PCI to local bus bridge (PCI PLX 9056) requires the pull-up/pull-down resistors provided on a system's main board.

Configuring or programming the FreeForm/PCI-104 in stand-alone mode is acceptable, providing that it is not left powered on in stand-alone state for an extended period of time.

WARNING	The power supply MSG037 included with the development kit DEV017 is intended for desktop programming only. It is not intended or warranted to be used in any other situation.

Software Installation

FPGA Development Environment

FreeForm/PCI-104 has been developed with Xilinx WebPACK 9.2, available free of charge at:

http://www.xilinx.com/ise/logic_design_prod/webpack.htm

PLX Software Development Kit (SDK)

PLX provides a software development kit (SDK) to aid in the creation of applications using the PLX 9056 bridge. The SDK provides a generic driver for Windows 2000/XP and Linux. A common API is also included; which encapsulates functions like:

- Configuration register read / write
- Block read / block write to local address space (i.e. memory / registers in the FPGA)
- Physical memory allocation, for bus mastering or DMA purposes
- Interrupt handling
- EEPROM read/write by address

The SDK is available for download from:

http://www.plxtech.com/products/sdk/

In order to download the SDK, you will need to register with PLX.

Reference Design & Application Examples

The FreeForm/PCI-104 ships with a CD containing:

- Documentation and manuals
- FPGA VHDL reference design
- Software program examples

The reference design and example programs help users quickly develop custom hardware and software applications. Refer to the CD for installation instructions.

The latest reference design is always available from:

http://devel.connecttech.com/

If a username and password have not already been provided, please contact Connect Tech Support via email support@connecttech.com.

FPGA Configuration

The Virtex-5 FPGA can be configured via two methods:

- JTAG programming chain, using P2
- SPI Flash, read on, power-up by FPGA

The configuration flash can be programmed (loaded) through three methods:

- JTAG programming chain (through FPGA), using P2
- Direct with cable, using P3 *[No longer supported after in ISE 12.x and later]*
- Indirect programming through FPGA, only possible after configuration is complete (refer to reference design for more details)

To configure the FPGA via the JTAG / boundary scan programming chain, three items are required:

- FPGA bitstream (*.bit), generated at end FPGA implementation using ISE
- PLX 9056 boundary scan definition file (*.bdsl)
- Ethernet PHY boundary scan definition file

To program the SPI flash, a hex file must be generated (*.mcs) then written to the flash. To generate the hex file, the following is required:

- FPGA Bitstream
- Setting PROM file format to MCS (important since bits are swapped)
- Setting SPI PROM density to 16M
- Setting SPI Flash type to M25P16

For a complete procedure, refer to Appendix A.

FPGA Ethernet MAC Addresses

The FreeForm/PCI-104's FPGA contains 2 dual Tri-Mode Ethernet MACs. One dual MAC is connected to the on-board Ethernet PHY, and the other is free for general use. In either case, the Ethernet MAC address is set by the user application, either HDL or embedded software – it is not hard coded as part of the FPGA silicon.

As such, the user is required to provide a valid Ethernet MAC address. If the end product usage is in the public domain, then this Ethernet MAC address must have a registered IEEE OUI designator.

If your organization or parent company does not have a registered IEEE OUI listing, please contact Connect Tech Inc. to obtain a valid Ethernet MAC address for your product.

Power and Thermal Considerations

The FreeForm/PCI-104's Virtex-5 FPGA is a versatile, flexible device, with many built-in features like termination, PLLs, and high speed gigabit transceivers. The drawback of these on-chip features is that they consume a lot of power and hence dissipate a lot of heat.

As a result Connect Tech, is recommending the installation of a heatsink, included with the product (see section Heat Sink Installation). As well, the FPGA designer *must* perform power analysis on their design to determine that they are not stressing the Virtex-5 component (i.e. exceeding the junction temperature).

Power analysis can be performed using the Xpower Analyzer (part of the ISE design suite) and the XPE spreadsheets (Xilinx Power Estimator Spreadsheets).

http://www.xilinx.com/products/design_resources/power_central/

Reference Design FPGA power analysis

Power analysis was performed on the FCG001 when configured with the reference design. The Virtex-5 XPE spreadsheet was used to determine an effective junction to ambient thermal resistance ($\theta_{JA_effective}$). The following parameters are entered into the spreadsheet to determine $\theta_{JA_effective}$.

Device	
Part	XC5VLX30T
Package	FF665
Grade	Industrial
Process	Typical
Speed Grade	-1
Stepping	Stepping - 1
Thermal Information	
Ambient Temp (°C)	50
Airflow (LFM)	250
Heat Sink	Custom
Custom ΘSA (°C/W)	8 (*)
Board Selection	Small (4"x4")
# of Board Layers	12 to 15

(θ_{SA} is the surface to ambient temperature for a heatsink with dimensions 27 mm x 27 mm x 6.4 mm and 250 LFM airflow. The θ_{SA} improves (decreases) with a taller heatsink.)

Three scenarios were developed and the XPE parameters Airflow and Custom ΘSA were varied. The $\theta_{JA_effective}$ was entered into the Xpower Analyzer yielding a Juction Temperature @ 50 °C and a maximum ambient temperature. The following table summarizes the scenarios and the results. For complete details of the scenarios, see Appendix B.

Scenario	**$\theta_{JA_effective}$ (°C/W)**	**$T_{ambient_max}$**	**$T_{junction}$ at 50 °C**
Heatsink attached, 250 LFM	4.9	82.7	67.3
No Heatsink, 250 LFM	6.4	72.7	72.7
No heatsink, 0 LFM	9.7	65.1	84.9

Calculation details:

$T_{junction} = T_{ambient} + (P_{FPGA} * \theta_{JA_effective}) = 50°C + (3.53W * 4.9\ °C\ /W) = 67.297°C$

$T_{ambient_max} = T_{junction_max} - (P_{FPGA} * \theta_{JA_effective}) = 100°C - (3.53W * 4.9\ °C\ /W) = 82.7°C$

Note $T_{junction_absolute_max}$ = 125°C is not used, since this is the absolute point of failure.

Specifications

Programmable FPGA	**Virtex-5 FPGA LX30T** **Virtex-5 FPGA LX50T** **Virtex-5 FPGA FX30T**
PCI-104 Bus	32 bit / 33 MHz 3.3V or 5V Signaling
Input Clock	100MHz
Memory / Flash	128MB DDR2-400 2MB or 4 MB Flash – FPGA configuration 8MB Flash – Embedded code 4K serial EEPROM – parameter storage
General Purpose User I/O	64 single ended I/O 32 LVDS I/O
Serial	2 x RS-485
Ethernet	2 x 10Base-T, 100Base-TX
High-speed serial	4 x Rocket I/O transceivers (GTP)
Operating Environment	Industrial Operating Temperature: -40°C to 85°C
Power Requirements	+5V DC 3.75 W (0.750 A @ 5V), average with standard reference design 0.75 W (0.150 A @ 5V), average with FPGA unconfigured
Dimensions	PC/104-*Plus* 2.2 compliant PCI-104 1.0 compliant 3.775” x 3.550”
Weight	85 g
Connectors	Two RJ-45 modular jacks (Ethernet) Two 2x5 0.100” headers (serial) One 2x40 0.050 x 0.100” header (general I/O) One 1x6 0.100” header (flash programming) One 2x14 0.8 mm differential pair terminal (high speed serial)

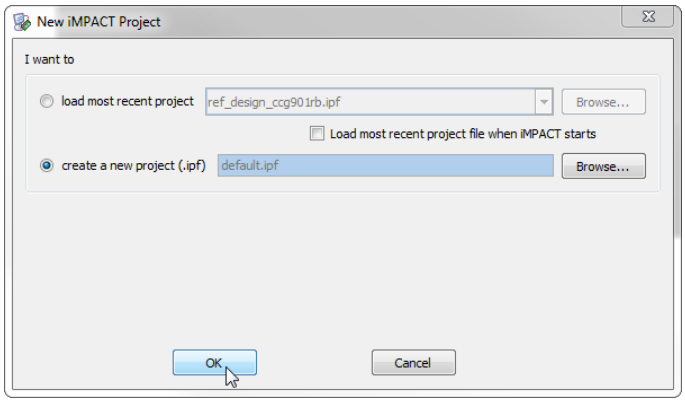
Appendix A: ISE iMPACT Procedures

IMPORTANT: As of the writing of this document, there are issues with Xilinx iMPACT in ISE 14.x when using in-direct programming of M25P## SPI flashes. It is recommended that you download ISE 13.4 lab tools to program the SPI flash. ISE 14.x can still be used for development and bitstream generation.

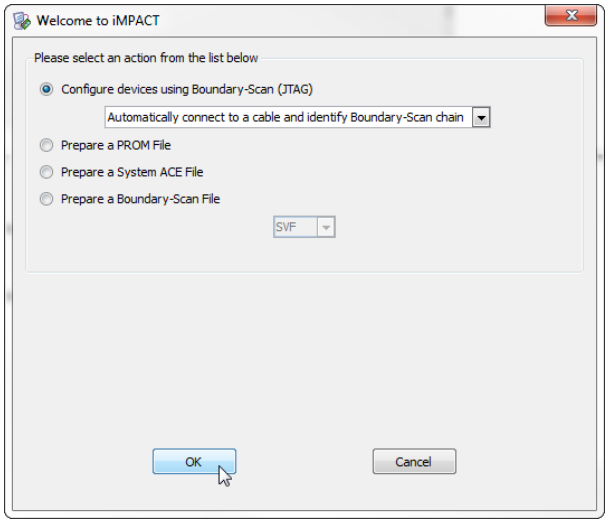
Preparing the iMPACT Project

1) Connect the JTAG programming cable to P2 ensuring that all JTAG signals align correctly.
   Note that P2 also has the TRST signal on pin 1, which is not part of Xilinx's Parallel or USB programming cables.

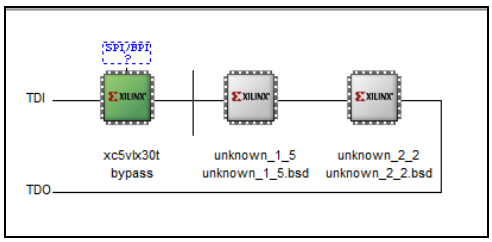
2) Open iMPACT, and select create a new project



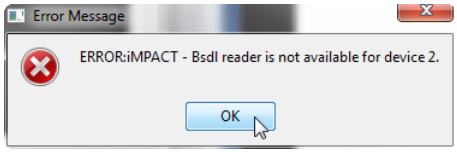
3) Select configure devices using boundary scan.



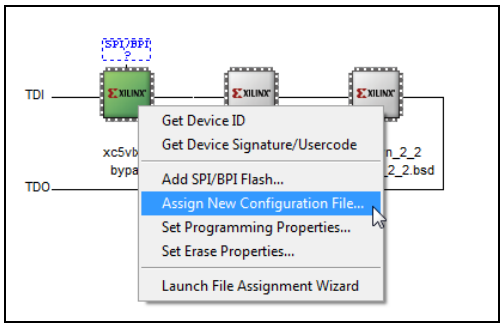
4) iMPACT will scan the JTAG chain, and identify three devices. The first device will be the FPGA.



5) When prompted with the following messages, click OK and Cancel



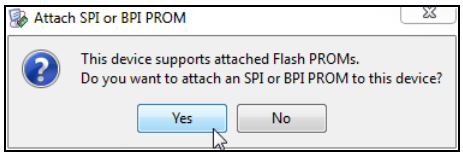
6) Right click on the FPGA, and click 'Assign new Configuration File'



7) Browse to the reference design directory, and select the bitstream (.bit)

Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ref_design.bit

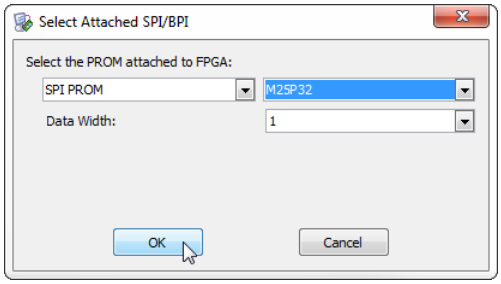
8) A prompt will ask if you wish to attach a SPI file or BPI Prom. Click Yes.



9) Browse to the reference design directory, and select the prom bile (.mcs)

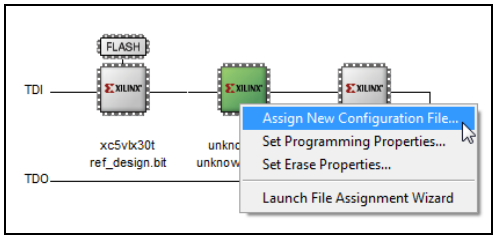
Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ ref_design_fcg001rd.mcs

10) A prompt will ask to select the attached SPI. Choose M25P32 and click ok



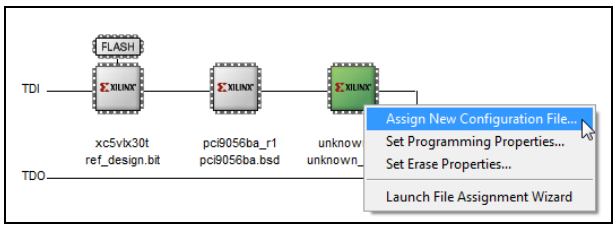
Note: Select "M25P16" (16 Mb flash) if using a FCG00x Rev B, FCG00x Rev C, or a FCG00x Rev D. with assembly Date 09/2009). To identify the flash size, refer to Appendix D: Identifying Configuration Flash Size

11) Right click on the second device in the JTAG chain and click 'Assign New Configuration File'



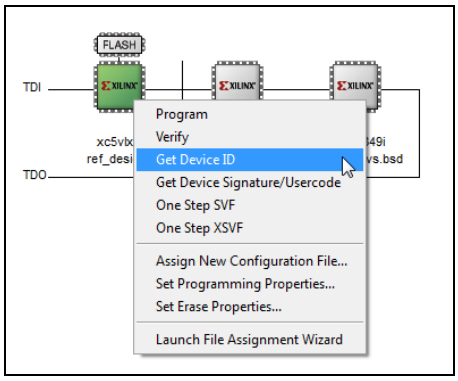
12) Browse to the bsdl folder and select PCI9056BA.bsd
Example: {REFDIR}\fpga\bsdl\PCI9056BA.bsd

13) Right click on the second device in the JTAG chain and click 'Assign New Configuration File'



14) Browse to the bsdl folder and select DP83849IVS.bsd.
Example: {REFDIR}\fpga\bsdl\ DP83849IVS.bsd

15) To test stream integrity, right click on the FPGA and select Get Device ID. The console will report 'Manufacturer's ID = Xilinx xc5vlx30t'




```
INFO:iMPACT - Current time: 2013-03-25 3:01:12 PM
// *** BATCH CMD : ReadIdcode -p 1
Maximum TCK operating frequency for this device chain: 10000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
'1': IDCODE is '11000010101001101110000010010011'
'1': IDCODE is 'c2a6e093' (in hex).
'1': : Manufacturer's ID = Xilinx xc5vlx30t, Version : 12
```

16) Save the iMPACT project (File -> Save Project As)
Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ ref_design_fcg001rd.ipf

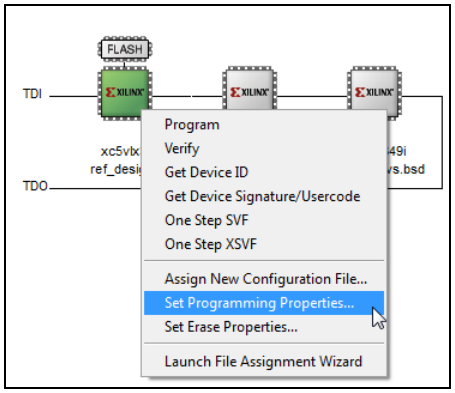
Programming the FPGA

1) Connect the JTAG programming cable to P2 ensuring that all JTAG signals align correctly.
Note that P2 also has the TRST signal on pin 1, which is not part of Xilinx's Parallel or USB programming cables.

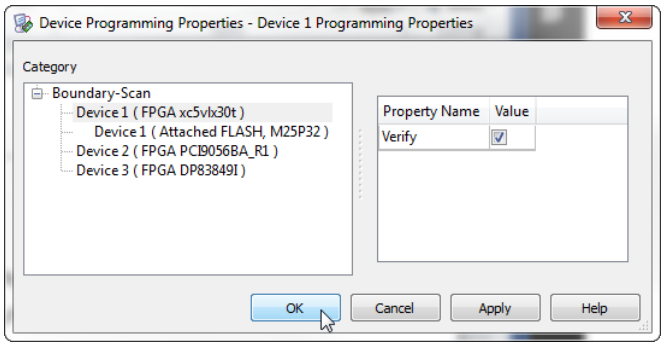
2) Remove all jumpers from J1; to ensure the flask is not loaded into the FPGA.

3) Open the recently saved iMPACT project file
Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ ref_design_fcg001rd.ipf

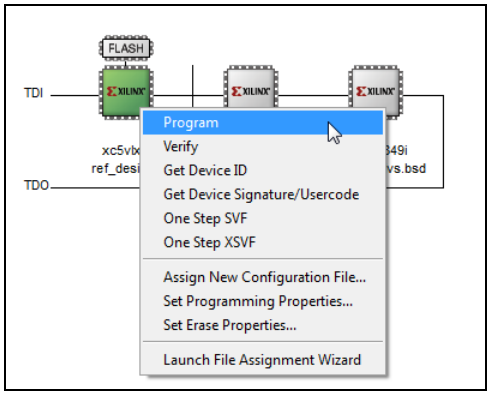
4) Right click on the FPGA and click 'Set Programming Properties'



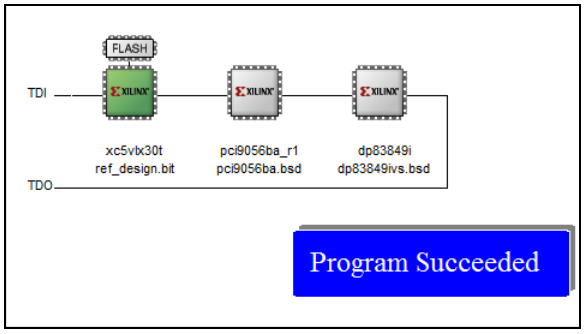
5) Select Device 1, check verify, and click OK



6) Right click on the FPGA and click 'Program'



7) Once the FPGA has been programmed successfully, you will see 'Program Succeeded'




```
INFO:iMPACT - Current time: 2013-03-25 4:49:45 PM
// *** BATCH CMD : Program -p 1 -v -dataWidth 1
PROGRESS_START - Starting Operation.
Maximum TCK operating frequency for this device chain: 10000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
'1': Programming device...
 Match_cycle = 2.
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1001 1110 0000 1010 1110 0000
 Match_cycle = 2.
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
'1': Verifying  device...INFO:iMPACT:2502 - Complete word count is
9363744/32=292617'.
INFO:iMPACT:2495 - Readback Size is 9363744.
done.
'1': Verification completed successfully.
 Match_cycle = 2.
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT:579 - '1': Completed downloading bit file to device.
INFO:iMPACT:188 - '1': Programming completed successfully.
 Match_cycle = 2.
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      6 sec.
```

8) Save the iMPACT project (File -> Save Project As)
Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ ref_design_fcg001rd.ipf

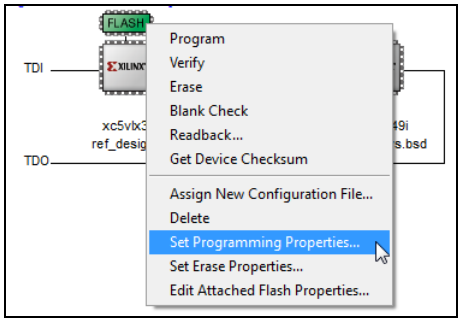
Programming the Flash

1) Connect the JTAG programming cable to P2 ensuring that all JTAG signals align correctly.
   Note that P2 also has the TRST signal on pin 1, which is not part of Xilinx's Parallel or USB programming cables.

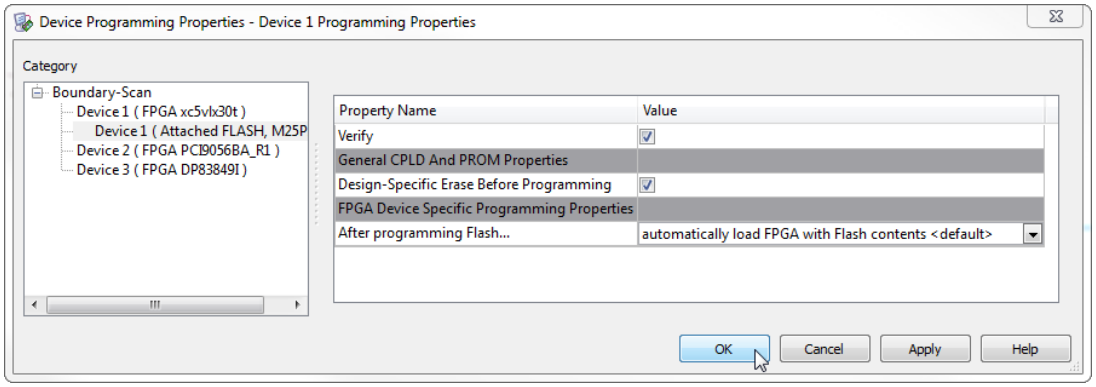
2) Add the appropriate jumper to J1.

3) Open the recently saved iMPACT project file
   Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ ref_design_fcg001rd.ipf

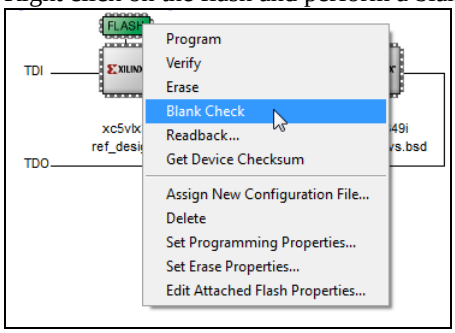
4) Right click on the flash, and click 'Set Programming Properties'



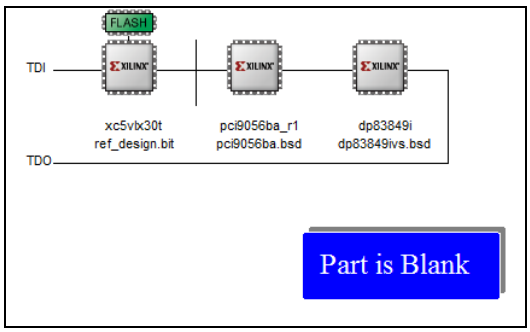
5) In Programming Properties dialog
   a. Check Verify
   b. Check Design specific Erase
   c. Select automatically load FPGA with Flash Contents
   d. Click OK



6) Right click on the flash and perform a blank check.

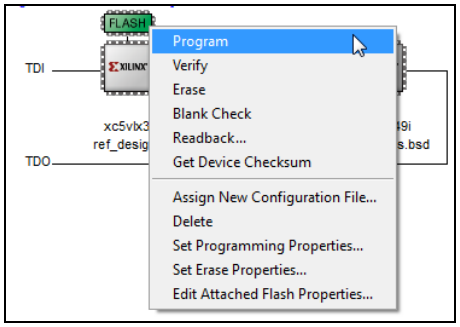


7) If the part is blank you will see:

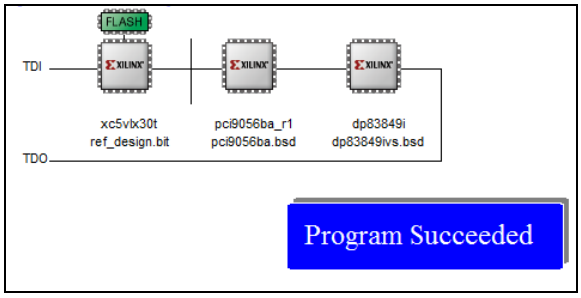



```
INFO:iMPACT - Current time: 2013-03-25 3:24:31 PM
// *** BATCH CMD : BlankCheck -p 1 -spionly
PROGRESS_START - Starting Operation.
Maximum TCK operating frequency for this device chain: 10000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
'1': IDCODE is '202016' (in hex).
'1': ID Check passed.
 '1': IDCODE is '202016' (in hex).
'1': ID Check passed.
 '1': Performing blank check on device...
'1': Part is blank.
PROGRESS_END - End Operation.
Elapsed time =     65 sec.
```

8) Right click on the flash and click ‘Program’



9) If the programming is succesful you will see:

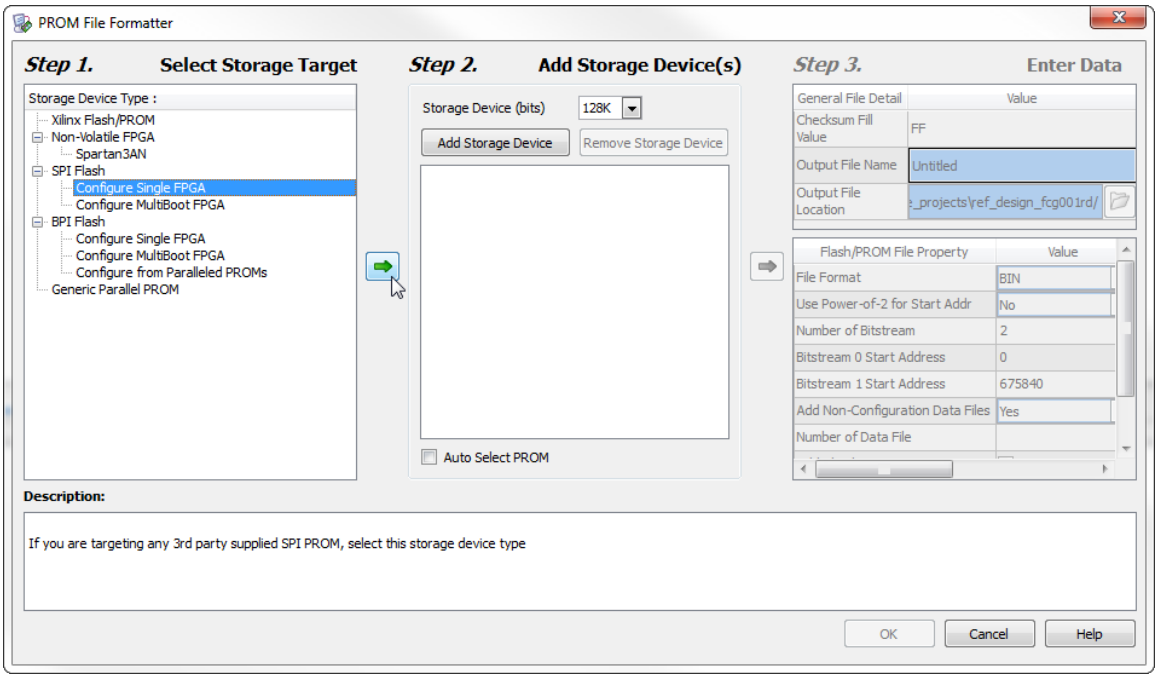



```
INFO:iMPACT - Current time: 2013-03-25 4:51:55 PM
// *** BATCH CMD : Program -p 1 -v -dataWidth 1 -spionly -e -v -loadfpga
PROGRESS_START - Starting Operation.
Maximum TCK operating frequency for this device chain: 10000000.
Validating chain...
Boundary-scan chain validated successfully.
1: Device Temperature: Current Reading: -273.00 C
1: VCCINT Supply: Current Reading:   0.000 V
1: VCCAUX Supply: Current Reading:   0.000 V
'1': SPI access core not detected. SPI access core will be downloaded to the
device to enable operations.
INFO:iMPACT - Downloading core file
C:/cad/Xilinx/13.4/LabTools/LabTools/virtex5/data/xc5vlx30t_spi.cor.
'1': Downloading core...
 Match_cycle = 0.
 LCK_cycle = NoWait.
LCK cycle: NoWait
done.
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1001 1110 0000 1010 1000 0000
INFO:iMPACT:2492 - '1': Completed downloading core to device.
'1': IDCODE is '202016' (in hex).
'1': ID Check passed.
 '1': IDCODE is '202016' (in hex).
'1': ID Check passed.
 '1': Erasing Device.
'1': Using Sector Erase.
'1': Programming Flash.
'1': Reading device contents...
done.
'1': Verification completed.
'1':Programming in x1 mode.
'1': Programmed successfully.
INFO:iMPACT - '1': Flash was programmed successfully.
 Match_cycle = 2.
 LCK_cycle = NoWait.
LCK cycle: NoWait
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =    167 sec.
```

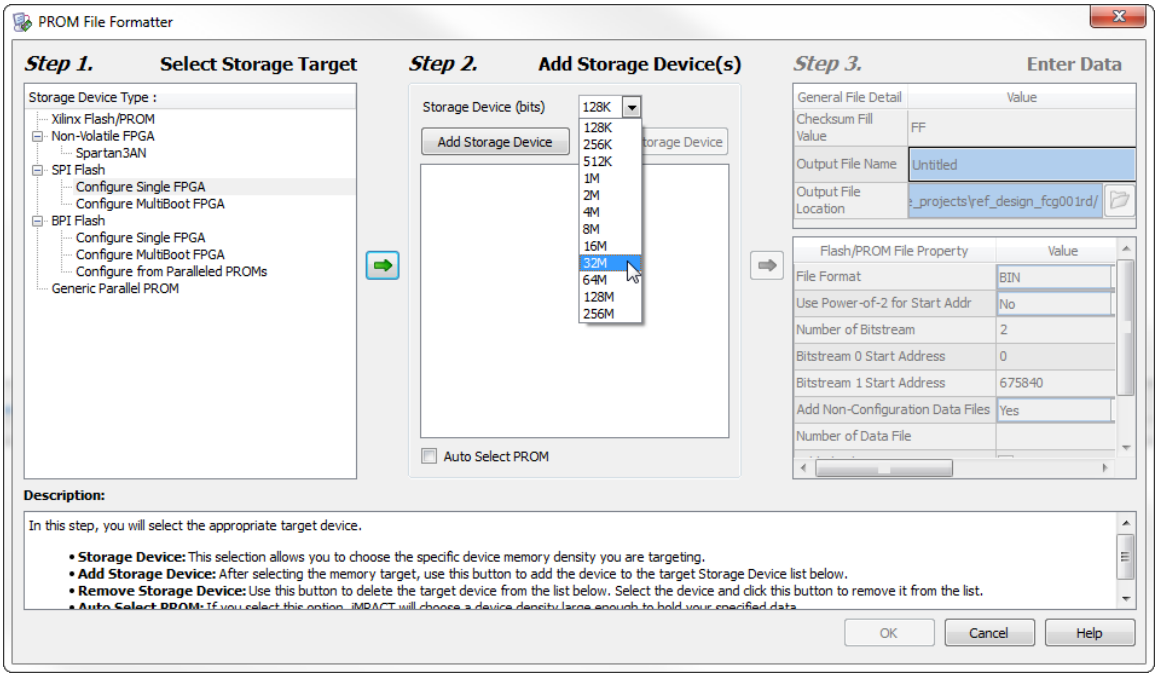
Generating a PROM (MCS) File

1) Double click PROM File Formatter in the Flows window.

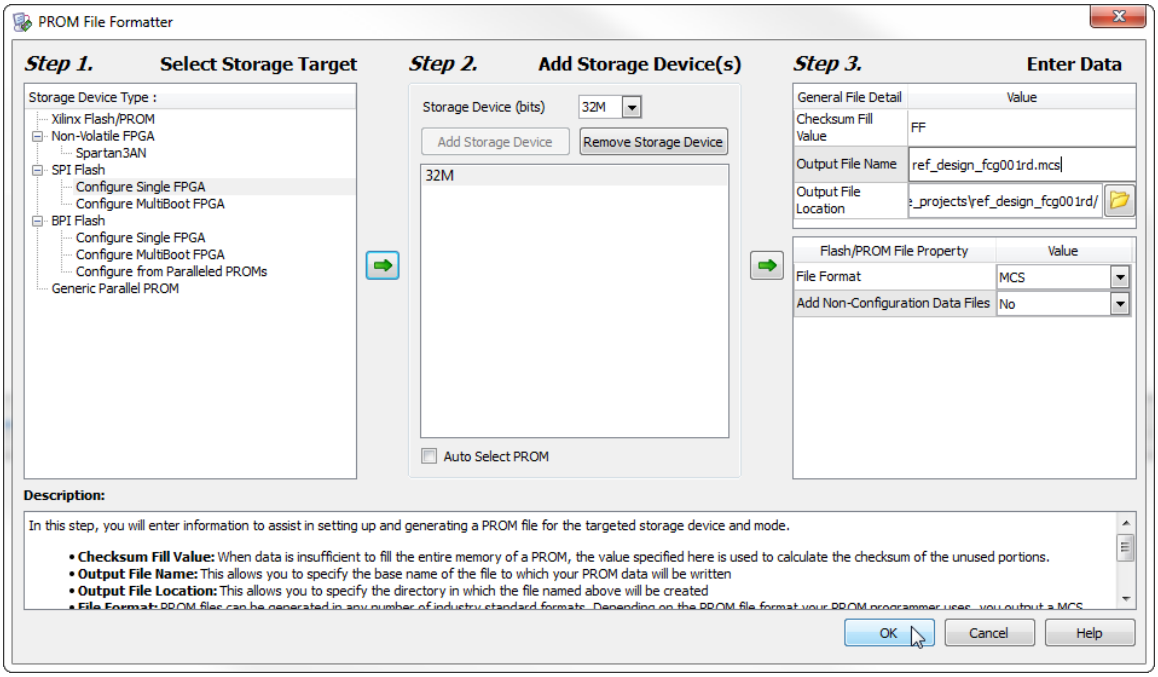
2) Select 'Configure Single FPGA', then click the green arrow



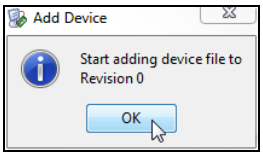
3) Select a storage device size of 32M (or 16M) then click the green arrow
Note: To identify the flash size, refer to Appendix D: Identifying Configuration Flash Size



4) Provide a name and location for the output mcs file, the click OK.



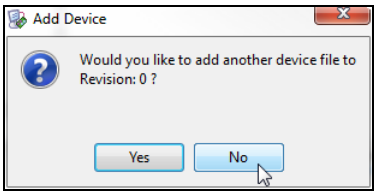
5) Click OK when prompted to add a new device

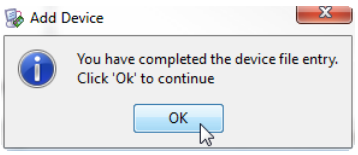


6) Browse to the reference design directory, and select the bitstream (.bit)

   Example: {REFDIR}\fpga\\ise_projects\ref_design_fcg001rd\ref_design.bit

7) When asked to add another device, click no, then click ok to complete the setup.





8) Under iMPACT processes, ‘click generate file’. This will produce 3 files:

   \fpga\\ise_projects\ref_design_fcg001rd\ref_design_fcg001rd.mcs
   \fpga\\ise_projects\ref_design_fcg001rd\ref_design_fcg001rd.prm
   \fpga\\ise_projects\ref_design_fcg001rd\ref_design_fcg001rd.cfi

Appendix B: Power calculations

Scenario 1: Heatsink attached, 250 LFM

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (W)	16	---	---
Logic	0.01646 (W)	3759	19200	19.6
Signals	0.05521 (W)	7757	---	---
IOs	2.06396 (W)	453	402	112.7
BRAMs	0.15807 (W)	23	36	63.9
DCMs	0.22787 (W)	3	4	75.0
GTP_DUALs	0.20747 (W)	2	4	50.0
TEMACs	0.00000 (W)	1	2	50.0
Total Quiescent Power	**0.66765 (W)**			
Total Dynamic Power	**2.86209 (W)**			
Total Power	**3.52974 (W)**			
Junction Temp	**67.3 (degrees C)**			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes	
Custom ThetaJA (degrees C/W)	4.9	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/W)	4.9	
Max Ambient (degrees C)	82.7	
Junction Temp (degrees C)	**67.3**	

Scenario 2: No Heatsink, 250 LFM

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (W)	16	---	---
Logic	0.01646 (W)	3759	19200	19.6
Signals	0.05521 (W)	7757	---	---
IOs	2.06396 (W)	453	402	112.7
BRAMs	0.15807 (W)	23	36	63.9
DCMs	0.22787 (W)	3	4	75.0
GTP_DUALs	0.20747 (W)	2	4	50.0
TEMACs	0.00000 (W)	1	2	50.0
Total Quiescent Power	**0.68723 (W)**			
Total Dynamic Power	**2.86209 (W)**			
Total Power	**3.54933 (W)**			
Junction Temp	**72.7 (degrees C)**			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes	
Custom ThetaJA (degrees C/W)	6.4	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/W)	6.4	
Max Ambient (degrees C)	77.3	
Junction Temp (degrees C)	**72.7**	

Scenario 3: No heatsink, 0 LFM

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (W)	16	---	---
Logic	0.01646 (W)	3759	19200	19.6
Signals	0.05521 (W)	7757	---	---
IOs	2.06396 (W)	453	402	112.7
BRAMs	0.15807 (W)	23	36	63.9
DCMs	0.22787 (W)	3	4	75.0
GTP_DUALs	0.20747 (W)	2	4	50.0
TEMACs	0.00000 (W)	1	2	50.0
Total Quiescent Power	**0.73730 (W)**			
Total Dynamic Power	**2.86209 (W)**			
Total Power	**3.59939 (W)**			
Junction Temp	**84.9 (degrees C)**			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes	
Custom ThetaJA (degrees C/W)	9.7	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/W)	9.7	
Max Ambient (degrees C)	65.1	
Junction Temp (degrees C)	**84.9**	

Appendix C: Hardware Changes from Revision B

This appendix lists the changes between hardware revision B and hardware revision C, D, E.
The following is a summary of changes:

- PCB requires only 5V over PCI-104; it previously required 3.3V and 5V
- A dedicated local bus oscillator was added to generate 50Mhz. A clock is no longer forwarded from FPGA to the PLX PCI 9056.
- The DDR2 FPGA pinout has been changed to increase timing margins
- The pinout of connector P4 (high-speed serial) has changed. The sideband signals have been relocated and 3.3V has been added.
- The orientation of connector P5 (RS-485 port 0) has rotated 180 degrees
- The Location of P8 (external power connector) has changed. The 3.3V enable signal has also been removed

Note: there are no functional or mechanical differences between Revision C, D, and E.

Reference Design

The top level reference design contains a generic parameter which will correctly configure the FPGA for Revision B or Revision C. A separate constraint file UCF is created for Revision B and Revision C/D/E, which need to be added to the ISE project manually.

Revision B

Local Clock Generation

Pin	Signal Name	
Y21	lb_lclkfb	Local clock generated in FPGA and forwarded to PLX bridge. Clock feedback to FPGA via pin Y21.
A20	lb_lclko_loop	
B21	lb_lclko_plx	

DDR2 Pinout

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AD21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC21	ddr2_dq<2>
Y7	ddr2_a<3>	AD14	ddr2_dq<3>
AB9	ddr2_a<4>	AE13	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AC8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AE17	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AC9	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AD24	ddr2_dq<16>
AE8	ddr2_cas_n	AE25	ddr2_dq<17>
AE11	ddr2_ck<0>	AC26	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AC23	ddr2_dq<19>
AD18	ddr2_cke<0>	AB22	ddr2_dq<20>
AC22	ddr2_cs_n<0>	AC24	ddr2_dq<21>
AE16	ddr2_dm<0>	AE26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD26	ddr2_dq<23>
AD25	ddr2_dm<2>	AD23	ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	ddr2_dq<25>
AD19	ddr2_dqs<0>	AF24	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF25	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD13	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

Revision C/D/E

Pin	Signal Name	
Y21	lb_lclkfb	Dedicated oscillator generates local bus clock. Clock is driven to FPGA on pin Y21, which drives an internal global clock net.
A20		
B21		

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AC21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC23	ddr2_dq<2>
Y7	ddr2_a<3>	AE13	ddr2_dq<3>
AB9	ddr2_a<4>	AD14	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AE8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AD21	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AD10	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AC26	ddr2_dq<16>
AC9	ddr2_cas_n	AE26	ddr2_dq<17>
AE11	ddr2_ck<0>	AC24	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AD24	ddr2_dq<19>
AC8	ddr2_cke<0>	AE25	ddr2_dq<20>
W8	ddr2_cs_n<0>	AB22	ddr2_dq<21>
AE16	ddr2_dm<0>	AD26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD25	ddr2_dq<23>
AE17	ddr2_dm<2>	AD23	Ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	Ddr2_dq<25>
AD19	ddr2_dqs<0>	AF25	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF24	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD9	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

Hardware Description

Connector Pinouts

High-speed Serial (P4)

The sideband LVCMOS signals (HSS) have been rearranged so that when two FreeForm units are connected:

HSS_USER_IO(0) maps to HSS_USER_IO(2)
HSS_USER_IO(1) maps to HSS_USER_IO(3)

Also, 3.3V pins replace the GND pins; this is because the connector has embedded GND blades.

Revision B

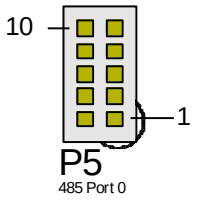
Pin	Signal
1	MTGRXN0_112
3	MTGRXP0_112
2	MTGTXN0_112
4	MTGTXP0_112
5	GND
7	GND
6	HSS_USER_IO(0)
8	HSS_USER_IO(1)
9	MTGRXN1_112
11	MTGRXP1_112
10	MTGTXN1_112
12	MTGTXP1_112
13	GND
15	GND
14	GND
16	GND
17	MTGRXN0_114
19	MTGRXP0_114
18	MTGTXN0_114
20	MTGTXP0_114
21	GND
23	GND
22	HSS_USER_IO(2)
24	HSS_USER_IO(3)
25	MTGRXN1_114
27	MTGRXP1_114
26	MTGTXN1_114
28	MTGTXP1_114

Revision C/D/E

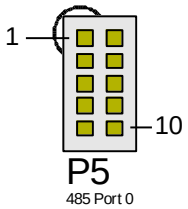
Pin	Signal
1	MTGRXN0_112
3	MTGRXP0_112
2	MTGTXN0_112
4	MTGTXP0_112
5	HSS_USER_IO(0)
7	HSS_USER_IO(1)
6	HSS_USER_IO(2)
8	HSS_USER_IO(3)
9	MTGRXN1_112
11	MTGRXP1_112
10	MTGTXN1_112
12	MTGTXP1_112
13	3.3V
15	3.3V
14	3.3V
16	3.3V
17	MTGRXN0_114
19	MTGRXP0_114
18	MTGTXN0_114
20	MTGTXP0_114
21	3.3V
23	3.3V
22	3.3V
24	3.3V
25	MTGRXN1_114
27	MTGRXP1_114
26	MTGTXN1_114
28	MTGTXP1_114

RS-485 Headers (P5)
The orientation of the connector has changed. The pinout remains the same.

Revision B



Revision C



External Power Connector (P8)
The connector no longer enables 3.3V regulation – it is always enabled.

Revision B

Pin	Signal
1	5V
2	3.3 enable (connect to 5V)
3	GND
4	VIO (connect to 5V)

Revision C/D/E

Pin	Signal
1	5V
2	
3	GND
4	VIO (connect to 5V)

Specifications

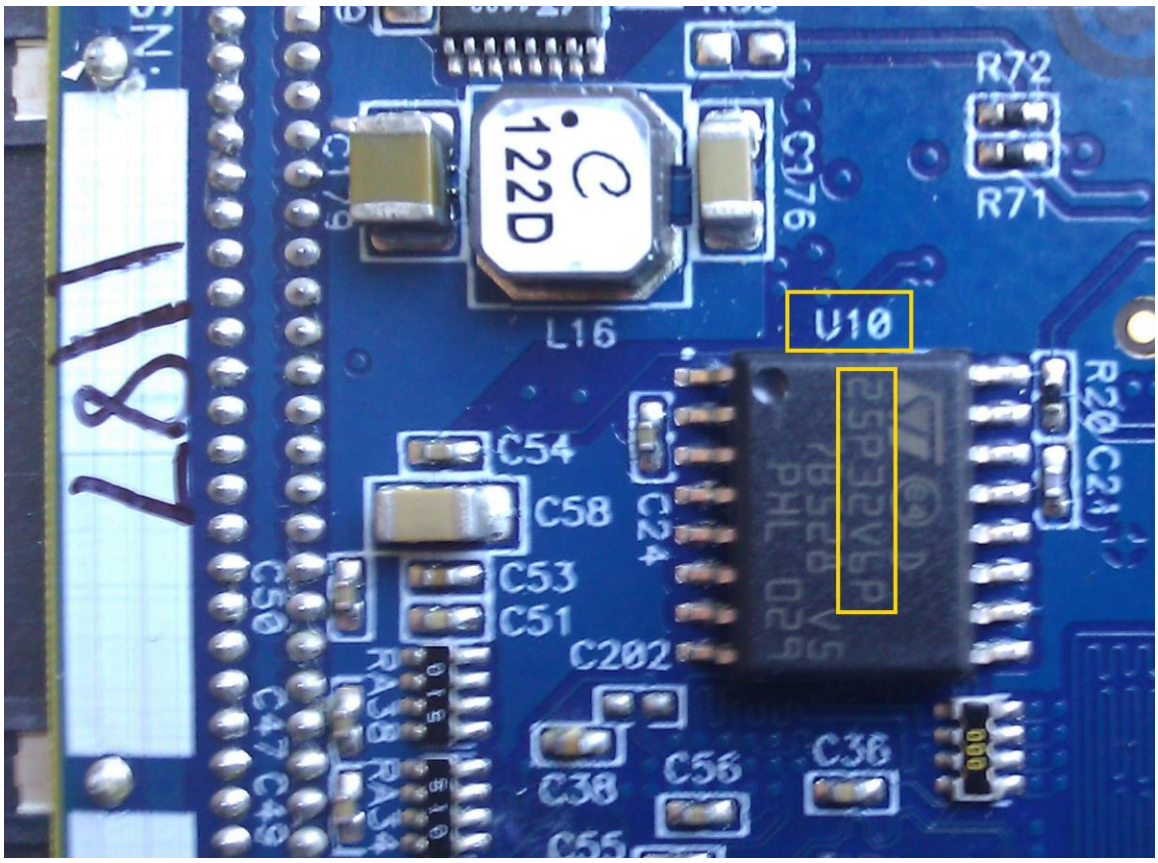
	Revision B	Revision C/D/E
Power Requirements	+3.3V DC and +5V DC, in PCI-104 stack +5V DC stand-alone Current requirements are configuration dependant.	+5V DC, in PCI-104 stack +5V DC stand-alone

Appendix D: Identifying Configuration Flash Size

The FreeForm/PCI104 is built with either

M25P32	32 Mbit	Rev D (> 09/2009), Rev E
M25P16	16 Mbit	Rev B, Rev C, Rev D (< 09/2009)

Both flash sizes are more than large enough to store a bitstream for any FreeForm/PCI104 variant. However, the correct flash size will need to be identified for programing.

To identify the flash, find U10 on the backside of the board and read the top side marking.

25P16 = M25P16 = 16 Mbit
25P32 = M25P32 = 32 Mbit