

Multi-IO FreeForm/104 Daughter Board

User Manual



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Customer Support Overview

If you experience difficulties after reading the manual and/or using the product, contact the Connect Tech reseller from which you purchased the product. In most cases the reseller can help you with product installation and difficulties.

In the event that the reseller is unable to resolve your problem, our highly qualified support staff can assist you. Our support section is available 24 hours a day, 7 days a week on our website at: www.connecttech.com/sub/support/support.asp. See the contact information section below for more information on how to contact us directly. Our technical support is always free.

Contact Information

We offer three ways for you to contact us:

Mail/Courier

You may contact us by letter at:
Connect Tech Inc.
Technical Support
42 Arrow Road
Guelph, Ontario
Canada N1K 1S6

Email/Internet

You may contact us through the Internet. Our email and URL addresses on the Internet are:

sales@connecttech.com
support@connecttech.com
www.connecttech.com

Note:

Please go to the [Download Zone](#) or the [Knowledge Database](#) in the [Support Center](#) on the Connect Tech website for product manuals, installation guides, device driver software and technical tips. Submit your technical support questions to our customer support engineers via the [Support Center](#) on the Connect Tech website.

Telephone/Facsimile

Technical Support representatives are ready to answer your call Monday through Friday, from 8:30 a.m. to 5:00 p.m. Eastern Standard Time. Our numbers for calls are:

Toll Free: 800-426-8979 (North America only)
Telephone: 519-836-1291 (Live assistance available 8:30 a.m. to 5:00 p.m. EST, Monday to Friday)
Facsimile: 519-836-4878 (on-line 24 hours)

Limited Lifetime Warranty

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Revision History

Revision 0.00 – June 15, 2012

Revision 0.01 – Jan. 28, 2015

Introduction

The Daughter Board is an adapter for Connect Tech's FreeForm/104 FPGA development board that enables users to capture and process synchronous and asynchronous RS232 or RS485/RS422 serial data with customizable FPGA implementations.

When used with a FreeForm/104 FPGA development board, the Daughter Board allows for easy and rapid design changes at run time, which makes it ideal for high speed, compute intensive, reconfigurable applications.

Connecting directly to the Digital I/O headers on the FreeForm/104, the Daughter Board also includes a PC/104 pass-through connector to allow the board to sit in-stack with the FreeForm/104 board.

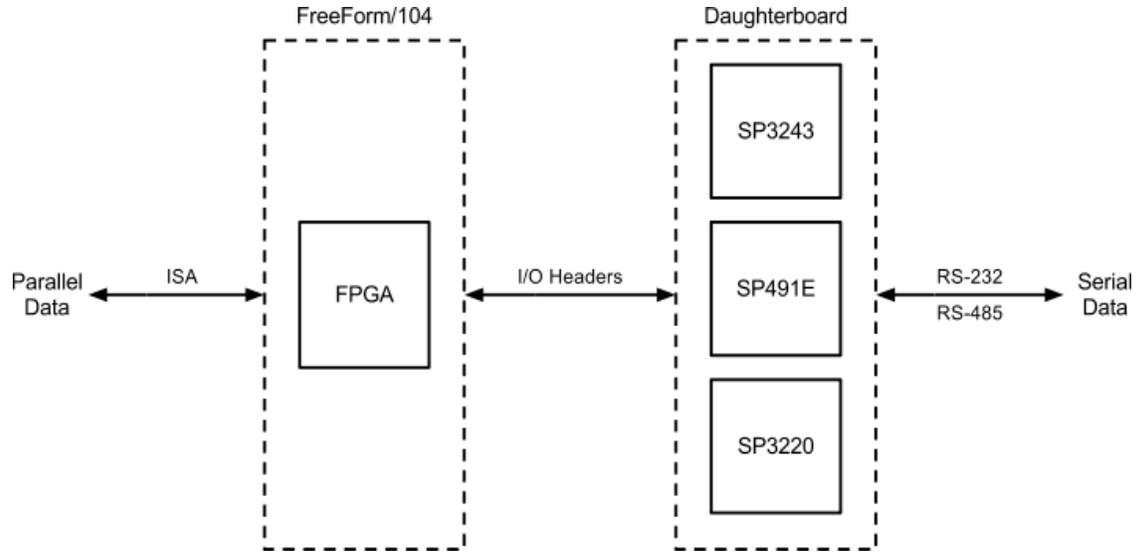
Features

- Integration with the FreeForm/104 Xilinx Spartan-3E FPGA enables UART design and data capture customization
- Two switchable RS-232, RS-422 or RS-485 channels, configurable to be fully synchronous or asynchronous
- Pass-through PC/104 connector allows the Daughter Board to stack with the FreeForm/104 parent-board

Specifications

Number of Ports	2
Electrical Interface	Synchronous RS-232, RS-422, RS-485
Control Signals	TxD, RxD, DTR, RTS, CTS, DCD, TxClk, RxClk
Connectors	PC/104 pass-through 2x50 pin connector to connect to FreeForm 2x26 pin header connectors (optional ribbon cables with female 26 pin IDC to female DB-26 connectors available)
Baud Rate	RS-232: Up to 1 Mbps Rs-422/RS-485: Up to 10 Mbps
Dimensions	Length: 14.699 cm/5.750" / 9.5885cm/3.775" Height: 11.049 cm/4.350" / 9.017cm/3.55"
Temperature	0°C to 70°C (-32°F to 159°F)
Bus	PC/104
Software Compatibility	Windows, Linux, QNX
System Requirements	Varies by configuration
Regulatory Approvals	FCC Class A EN50082-2 ICES-003 Class A EN550022 Class A EN55024
Warranty and Support	Lifetime warranty and free technical support

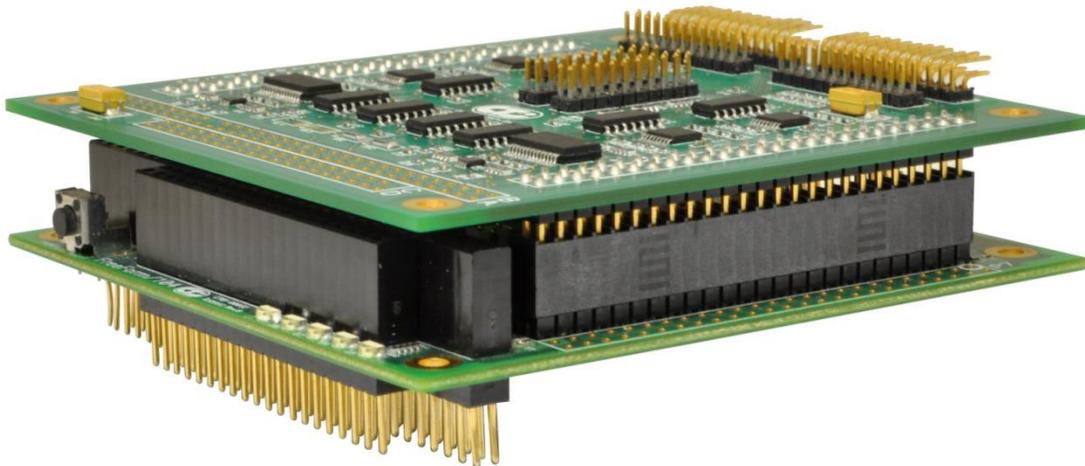
System Block Diagram



Hardware Installation Information

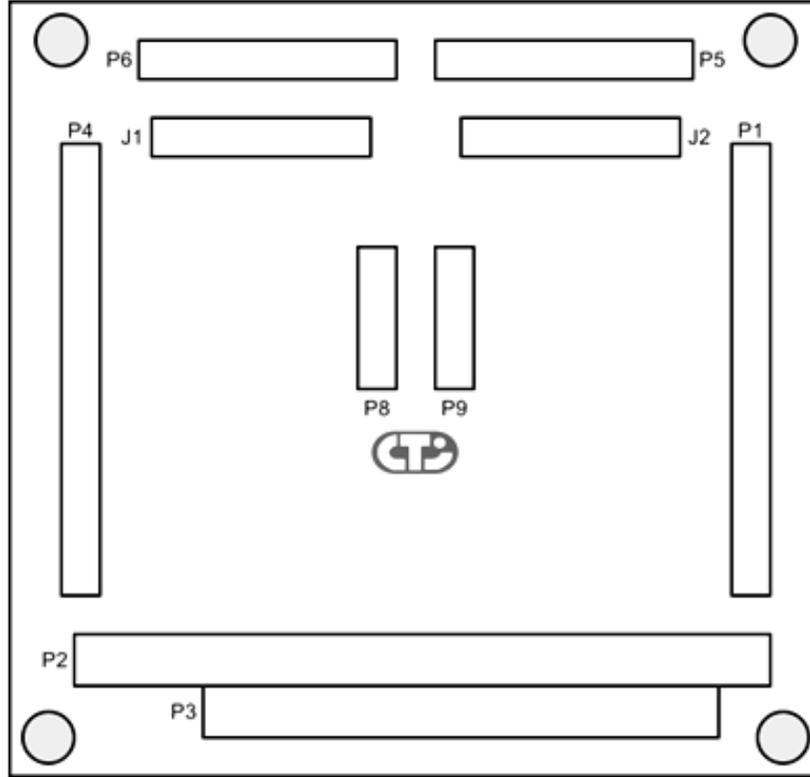
Please follow these steps with installing the Daughter Board into your system.

- 1) Ensure your FreeForm/104 is powered OFF
- 2) Install the Daughter Board onto the FreeForm/104
- 3) Power ON your FreeForm/104



Hardware Description

Board Diagram



Connector Summary

Location	Connection
P1, P4	FreeForm/104 Header Connectors
P2, P3	Pass-through PC/104 Connectors
P5	Port 2 Serial I/O
P6	Port 1 Serial I/O

Jumper Summary

Location	Connection
J1	Port 1 Mode Selection Jumpers
J2	Port 2 Mode Selection Jumpers
P8	Port 1 Control Line Jumpers
P9	Port 2 Control Line Jumpers

Daughter Board to FreeForm/104 Pin Interconnect

The Daughter Board connects directly to the Digital I/O headers on the FreeForm/104. The following table lists the pin interconnect:

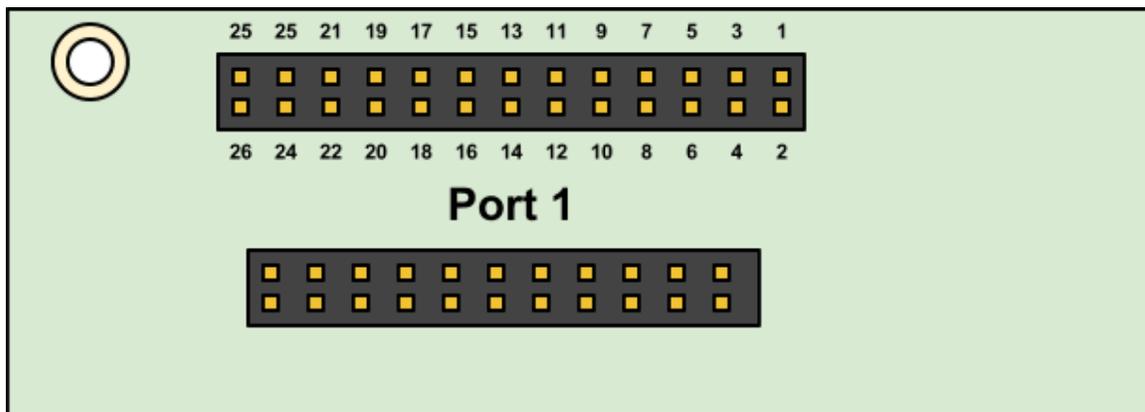
Signal	P8 Header Pin (Daughter Board Port 1)	Freeform Signal	FreeForm Register
TX1	1	DIO_2A7	8255 2 Port C I/O
RTS1	3	DIO_2A6	8255 2 Port C I/O
DTR1	5	DIO_2A5	8255 2 Port C I/O
RX1	2	DIO_3A7	8255 3 Port C I/O
CTS1	4	DIO_3A6	8255 3 Port C I/O
DSR1	6	DIO_3A5	8255 3 Port C I/O
DCD1	8	DIO_3A4	8255 3 Port C I/O
RI1	10	DIO_3A3	8255 3 Port C I/O
TXC1	17	DIO_2B7	8255 2 Port B I/O
RXC1	18	DIO_3B7	8255 3 Port B I/O

Signal	P6 Header Pin (Daughter Board Port 2)	Freeform Signal	FreeForm Register
TX2	1	DIO_0C7	8255 0 Port A I/O
RTS2	3	DIO_0C6	8255 0 Port A I/O
DTR2	5	DIO_0C5	8255 0 Port A I/O
RX2	2	DIO_1C7	8255 1 Port A I/O
CTS2	4	DIO_1C6	8255 1 Port A I/O
DSR2	6	DIO_1C5	8255 1 Port A I/O
DCD2	8	DIO_1C4	8255 1 Port A I/O
RI2	10	DIO_1C3	8255 1 Port A I/O
TXC2	17	DIO_0B7	8255 0 Port B I/O
RXC2	18	DIO_1B7	8255 1 Port B I/O

Output Pin Reference

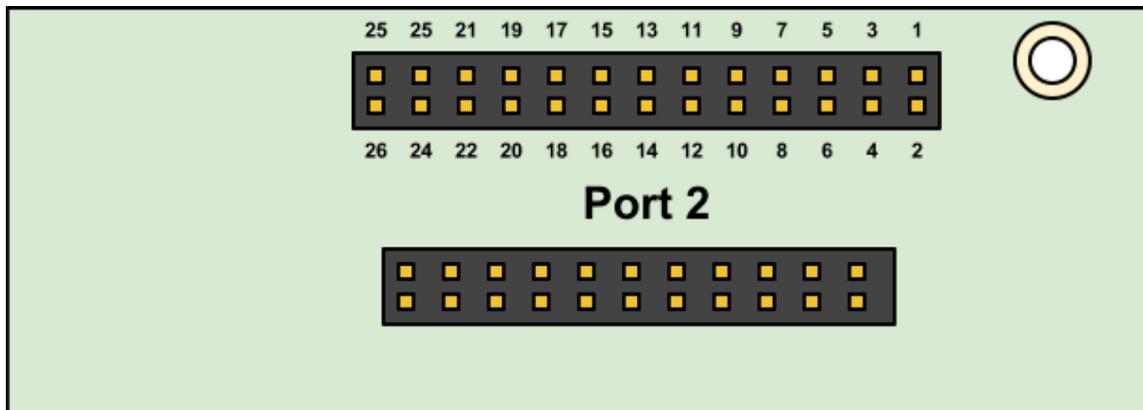
Port 1

Pin	Description
1	GND
2	TX1+
3	TX1-
4	TXCI-
5	RX1-
6	RX1+
7	RTS1-
8	RXCI-
9	CTS1-
10	
11	DSR1-
12	RTS1+
13	GND
14	DTR1-
15	DCD1-
16	
17	RXCI+
18	
19	
20	
21	
22	
23	TXCI+
24	RI1-
25	CTS1+
26	



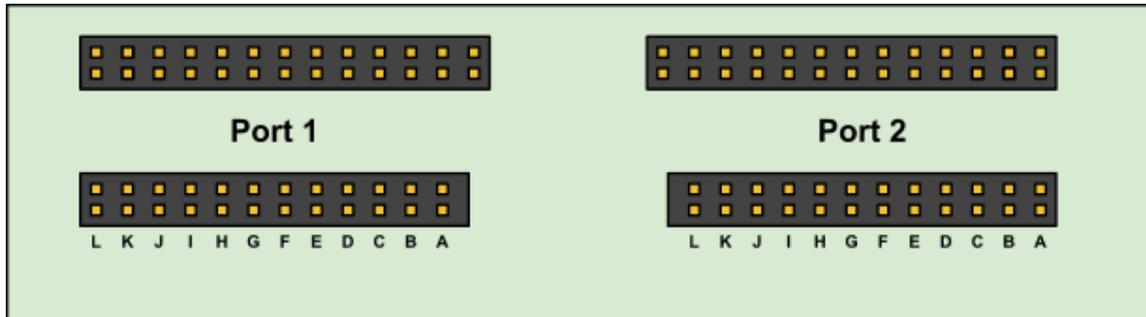
Port 2

Pin	Description
1	GND
2	TX2+
3	TX2-
4	TX2I-
5	RX2-
6	RX2+
7	RTS2-
8	RXC2-
9	CTS2-
10	
11	DSR2-
12	RTS2+
13	GND
14	DTR2-
15	DCD2-
16	
17	RXC2+
18	
19	
20	
21	
22	
23	TXC2+
24	RI2-
25	CTS2+
26	



Mode Selection Jumper Reference

The following diagram shows the mode selection jumper locations for both Port 1 and Port 2. Jumpers are placed vertically, connecting the two pins located directly above the corresponding letter:



Jumper Selection Key for Port Modes

A	B	C	Mode
Out	Out	Out	RS232
In	Out	Out	RS485 FD
In	In	Out	RS485 MDS (TX Control)
In	In	In	RS485HD (TX/RX Control)
In	Out	In	Undefined (RX Control)

*Note: this jumper solution/layout was taken from the BlueStorm Family

Clock Bias / Termination Jumper Selections

D	E	F	Result
X	X	Out	No Tx Termination
X	X	In	Tx Terminated
Out	Out	X	No Rx Bias/Termination
In	In	X	Rx Bias/Termination Enabled

G	H	I	J	Result
Out	Out	Out	Out	No Termination/Bias
In	In	Out	Out	Tx Clock Termination/Bias
Out	Out	In	In	Rx Clock Termination/Bias
In	In	In	In	Rx/Tx Clock Termination/Bias

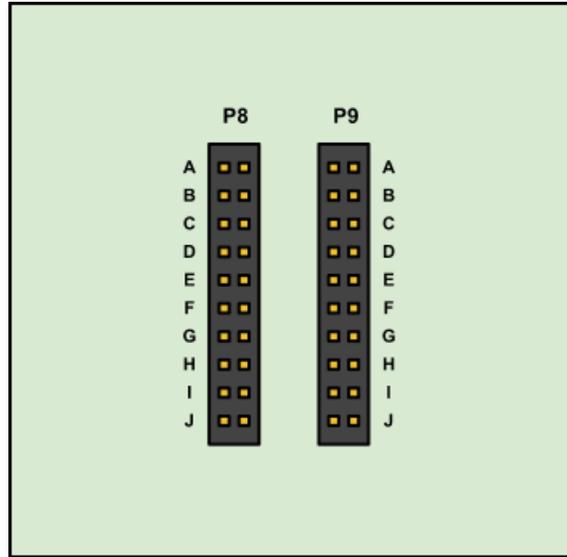
Clock Combination Jumper Selections

K	L	Result
In	In	Clocks are Combined
Out	Out	Clocks are Separate

*Note: when combining clocks, it is best to disable one of the transceivers

Control Line Jumper Reference

The following diagram shows the control line jumper locations for both Port 1 and Port 2 (P8 and P9 respectively). Jumpers are placed horizontally, connecting the two pins located directly beside the corresponding letter:



RS-232 Clock Signals

SP3220 transceivers are used to accomplish the bidirectional signalling needed. These are single driver, receiver transceivers with the ability to individually tri-state the driver or receiver or both. This allows for shared signal lines, with the intention that only one section of the part is active at a time.

The Shutdown and Enable pins on the 3220 are used to create the tri-stating:

SH	EN	TX-Out	RX-OUT	Result
0	0	Tri-State	Active	Receiver Only
0	1	Tri-State	Tri-State	Both Disabled
1	0	Active	Active	Both Enabled (Avoid)
1	1	Active	Tri-State	Driver Only

Because the daughterboard is configured to have both driver and receiver disabled by default, the SH pin can be used as the Driver enable while the EN pin can be used as the receiver enable.

This leaves the following jumper setup:

Jumper	Result
C	TX Clock as receiver
D	TX Clock as driver
G	RX Clock as receiver
H	RX Clock as driver

The state where both driver and receiver are enabled should be avoided as the behaviour of the chip is unknown in this state.

RS-485 Clock Signals

These signals are configured in a similar method to the 232 signals, with the SP491 chips being used. These chips also have individual enables for both the driver and receiver. The receiver enable is active low, while the driver is active high. Like 232, both driver and receiver are defaulted off by the daughter board.

This leaves the following jumper setup:

Jumper	Result
E	TX Clock as receiver
F	TX Clock as driver
I	RX Clock as receiver
J	RX Clock as driver